An Implementation of Real-time and Parallel Processing ECG Features an Extraction Algorithm in a Field Programmable Gate Array (FPGA)

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For a homecare electrocardiogram (ECG) monitoring device, it is important to extract the features of the signal in real-time. The objective of this abstract is to report a successfully development of a parallel processing, real-time ECG features extraction algorithm that could be implemented using Field programmable Gate Array (FPGA) device. The implemented System on Chip (SOC) using FPGA that could be used to acquire digital ECG data from an Analog-to-Digital Converter (ADC), to display ECG and extracted information on a VGA type LCD device, to store the acquired ECG and the extracted information into a flash memory chip and to communicate to a PC computer using an USB device. The hardware implementing algorithm was developed in Verilog Hardware Description Language (HDL). It will be analyzing the component of the ECG signals and extracted 12 features of ECG information in real time within two heart beats. The system will be using these features primarily to identify the abnormal rhythm of heart beat. The prototype system has been tested in real-time. The performance of algorithm was tested and validated using the MIT-BIH Arrhythmia annotated database against the result from MATLAB. This overall average R-peak timing detection difference against the annotated data (250Hz) to the algorithm data was 0.25 ± 0.44 sampling point and is 0.001 ± 0.0018 seconds. For timing of Q-peak detection difference, it was -2.05 ± 1.76 sampling points. And, the system has been tested to acquire ECG signals and the features extracted from five volunteers in real-time and on line.